Digital Logic Design

Course Code: EE-223	**Credit Hours:** 2-1

Course Description

Digital Logic Design is a one-semester course taken by Computer Science students during first year of their bachelor's program. This course introduces the logic operators and gates to lay the framework for strengthening the basic understanding of computer building blocks. Both combinational and sequential circuits are studied in this course along with their constituent elements comprising Arithmetic circuits, Comparators, Decoders, Encoders, Multiplexers, Tri-state buffers as well as Latches, Flip-flops, Counters and Registers. In this course students will learn principles of Digital Logic Design. They will combine classical design methodologies with a series of laboratory assignments in which they will demonstrate their ability to successfully design, implement, and debug digital systems using Computer Aided Design tools and physical prototyping.

Text Book:

1. Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog (Sixth Edition) by M. Morris Mano and Michael Ciletti

Reference Book:

1. Digital Fundamentals (Eleventh Edition) by Floyd
2. Logic and Computer Design Fundamentals (4 th Edition) by M. Morris Mano and Charles R. Kime

Prerequisites

None

ASSESSMENT SYSTEM FOR THEORY

Quizzes	15%
Assignments	05%
Mid Terms	30%
ESE	50%

ASSESSMENT SYSTEM FOR LAB

Quizzes	10%-15%
Assignments	5% - 10%
Lab Work and Report	70-80%
Lab ESE/Viva	20-30%

Teaching Plan

Week No	Topics	Learning Outcomes
1	Introduction	Digital Systems and motivation for study. Number Systems: Binary, Octal, Decimal and Hexadecimal Numbers and Base Conversions.
2-8	DLD-I	Complements: Subtraction of Unsigned Numbers using Complements. Familiarization of Basic Gates and Digital ICs, Signed Binary Numbers Arithmetic: Addition and Subtraction of Signed Numbers. Binary Codes. Binary Logic: Definition of Binary Logic and Logic gates. Boolean Algebra: Basic and Axiomatic Definition of Boolean Algebra; Two-Valued Boolean Algebra. Basic Theorems and Properties of Boolean Algebra. Boolean Functions; Canonical and Standard Forms. The K-Map Method; Two, Three, and Four - Variable K- Maps. Sum-ofProducts (SOP) simplification using K-Map. Essential and Non-essential Prime Implicants. Product- of- Sums (POS) Simplifications using K-map. Don't Care conditions. Quine-McCluskey Minimization algorithm (Tabulation method). NAND and NOR implementations. Combinational Circuits: Design Procedure with Code Conversion Example. Design of 4-BIT Ripple Carry and Carry Look-ahead Adder-Subtractor using Full Adders, Overflow
9	**MID TERM IN WEEK 9**	

10-17	DLD-II	Design of a 2-bit Adder/Subtractor Circuit. Combinational Logic Design using Verilog HDL. Magnitude Comparator, Decoders/Demultiplexers. Encoders and Multiplexers. Tri-State Gates. And their applications. Storage Elements: Flip-Flops, Other FlipFlops, Conversion of Flip-Flops. Analysis of Clocked-Sequential Circuits; State Equations, State Table, State Diagram, and Flip-Flop input equations. Analysis with D Flip-Flops, JK Flip-Flops, and T Flip-Flops. Mealy and Moore Models. State Reduction using Row Matching Method. State Assignment. State Reduction using Row Matching and Implication Table Techniques. Design Procedure Synthesis using D Flip-Flops, JK Flip-Flops, and T Flip-Flops. Shift Registers; 4-Bit Shift Register; Serial Transfer and Serial Addition. 4-Bit Universal Shift Register. Ripple Counters; Binary and BCD Ripple Counters. Synchronous Counters; Binary and BCD Counters.
18	**FINAL TERM IN WEEK 18**	

Practical:

Experiment No	Description
1	Familiarization of Basic Gates and Digital ICs
2	Introduction to Verilog HDL. Basic language constructs and design entry using Verilog HDL.
3	Derivation of Boolean Functions from given logic diagram and its Hardware implementation. Function implementation using Verilog HDL
4	Minimization of Boolean Functions and its Hardware implementation.
5	Design of Binary-to-Gray/Gray-to-Binary Code Converter using basic gates. Gate-Level Modeling of Combinational Circuits using Verilog HDL.
6	BCD-to-Seven Segment Decoder Design
7	Design of a 2-bit Magnitude Comparator using Classical design method. Combinational Logic Design using Verilog HDL.
8	Design of a 2-bit Adder/Subtractor Circuit.Combinational Logic Design using Verilog HDL.
	MID TERM IN WEEK 9
10	Design of 4-bit ALU.
11	Voting Machine Design
12	Memory Elements: Latches and Flip-flops. Design of a positive-edge triggered D flip-flop. Sequential Logic Design using Verilog HDL

13	Flip-Flop Applications & Proteus Simulation of Digital Circuits
14	Sequence Detector Design. Sequential Logic Design using Verilog HDL
15	**Open-Ended Lab**
16	**Open-Ended Lab**
17	**Final Lab**
18	**FINAL TERM IN WEEK 18**